Facilitating Spectrum Access by Noise Guessing

Arslan Riaz[1], Furkan Ercan[1], Zeynep Ece Kizilates[1], Akshaya Bali[1], Alperen Yasar[1], Kevin Galligan[3], David Starobinski [1], Ken R. Duffy[4], Muriel Medard[2], Rabia Tugce Yazicigil[1]

PI : Muriel Medard[2], David Starobinski [1], Rabia Tugce Yazicigil[1]

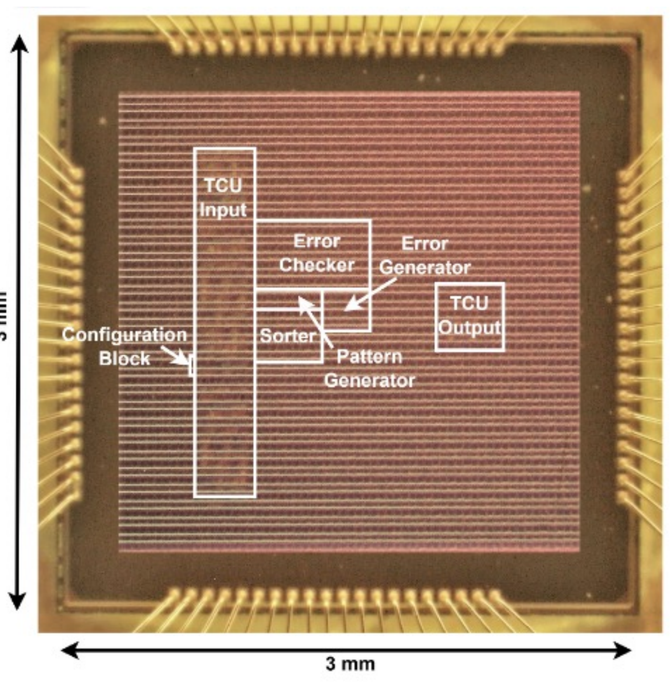
[1]Department of Electrical & Computer Engineering Boston University, Boston, MA, [2]Department of Electrical Engineering and Computer Science Massachusetts Institute of Technology, Cambridge, MA, [3]Hamilton Institute, Maynooth University, Maynooth, Ireland,
[4]Department of Electrical and Computer Engineering & Department of Mathematics, Northeastern University, Boston, MA, USA

Award Numbers: 2128517 (https://www.nsf.gov/awardsearch/showAward?AWD_ID=2128517), 2128555 (https://www.nsf.gov/awardsearch/showAward?AWD_ID=2128555&HistoricalAwards=false)

Motivation

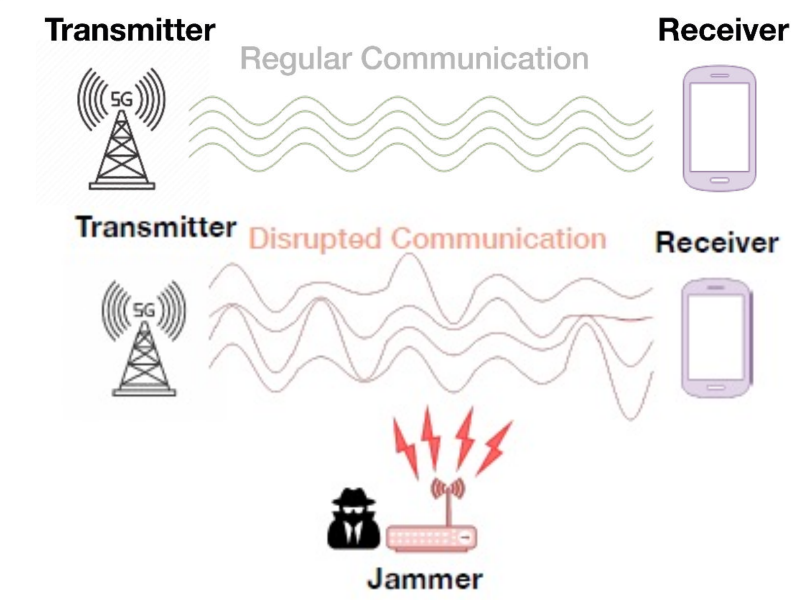
This project investigates cross-layer optimization of hardware, algorithms, and systems to address spectrum utilization and sharing challenges, including energy efficiency and security. Toward this goal, we introduced the first integrated **universal** soft-detection decoder using ORBGRAND.

- Decode any short-length and high-rate codes
- At target FER 10^{-7}
  - Ultra-low energy consumption of 0.76pJ/bit
  - Lowest power consumption of 4.9mW
  - Comparable throughput of 6.5Gbps
- Decoder performance is independent of the codebook
- Dynamically adapts to the channel noise conditions



Interference and Jammers

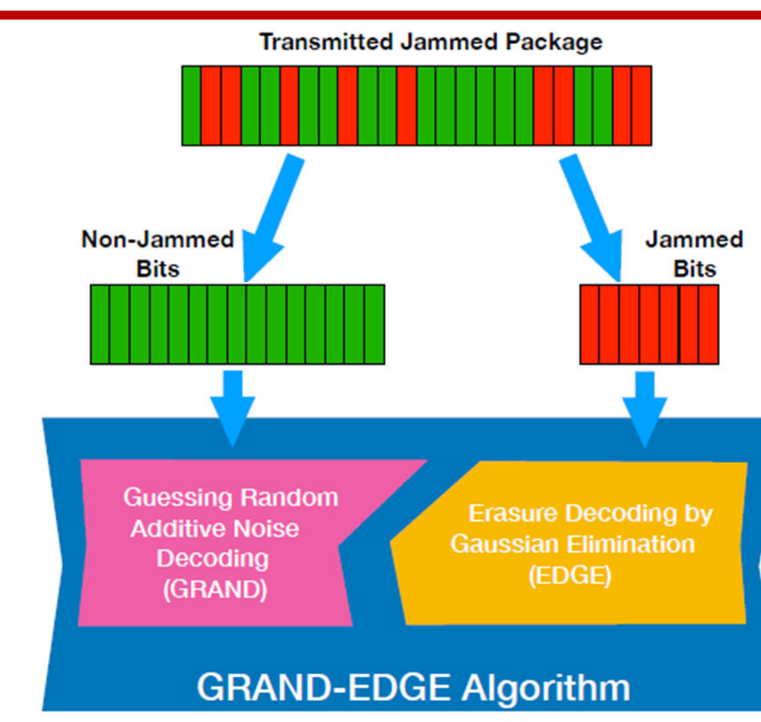
- Interference and jammers disrupt communication severely
- Channel signal strength indicators can easily detect anomalies but cannot help recover transmitted data
- Disruption causes re-transmission with overhead in latency and power consumption
- **GRAND-EDGE adds resilience against jamming events**



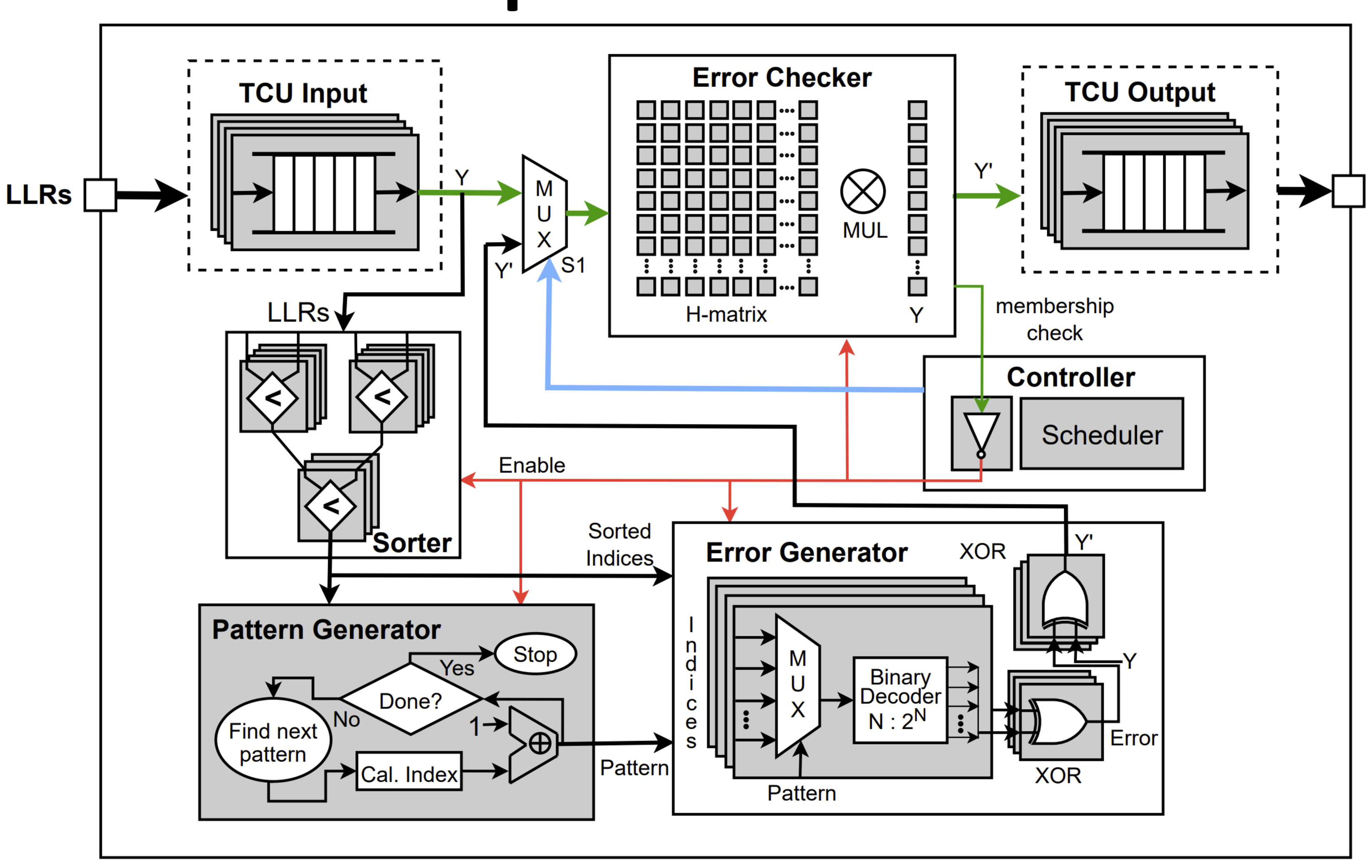
GRAND-EDGE Algorithm

We introduced a jamming-resilient algorithm leveraging GRAND:

- **Step 1**: Identify and separate jammed bits from unjammed bits
- **Step 2-GRAND:** Perform error correction on unjammed bits
- **Step 3-EDGE Subroutine:** Estimate values of jammed bits through Gaussian Elimination

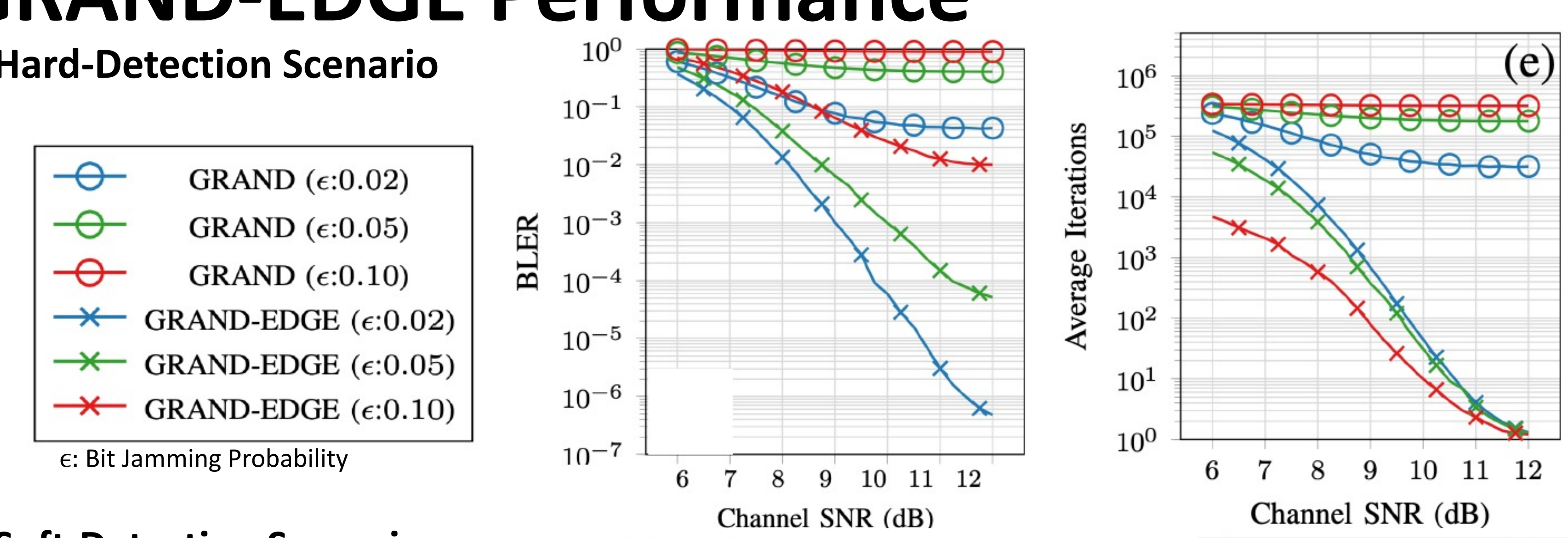


ORBGRAND Chip Architecture

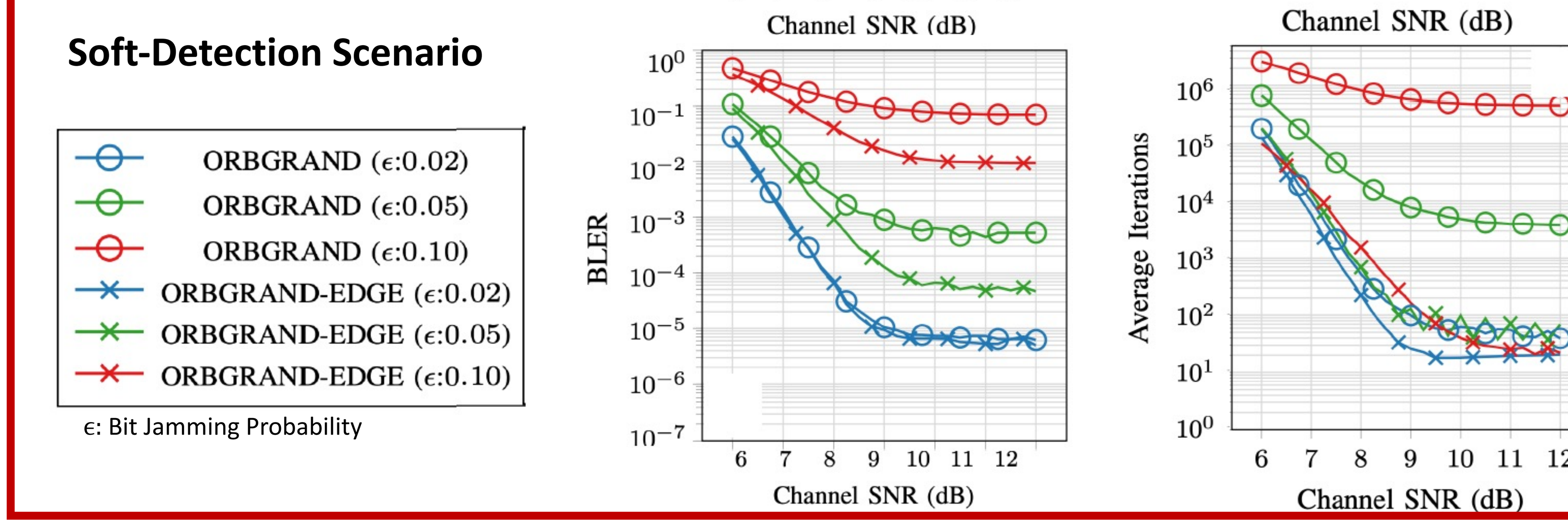


GRAND-EDGE Performance

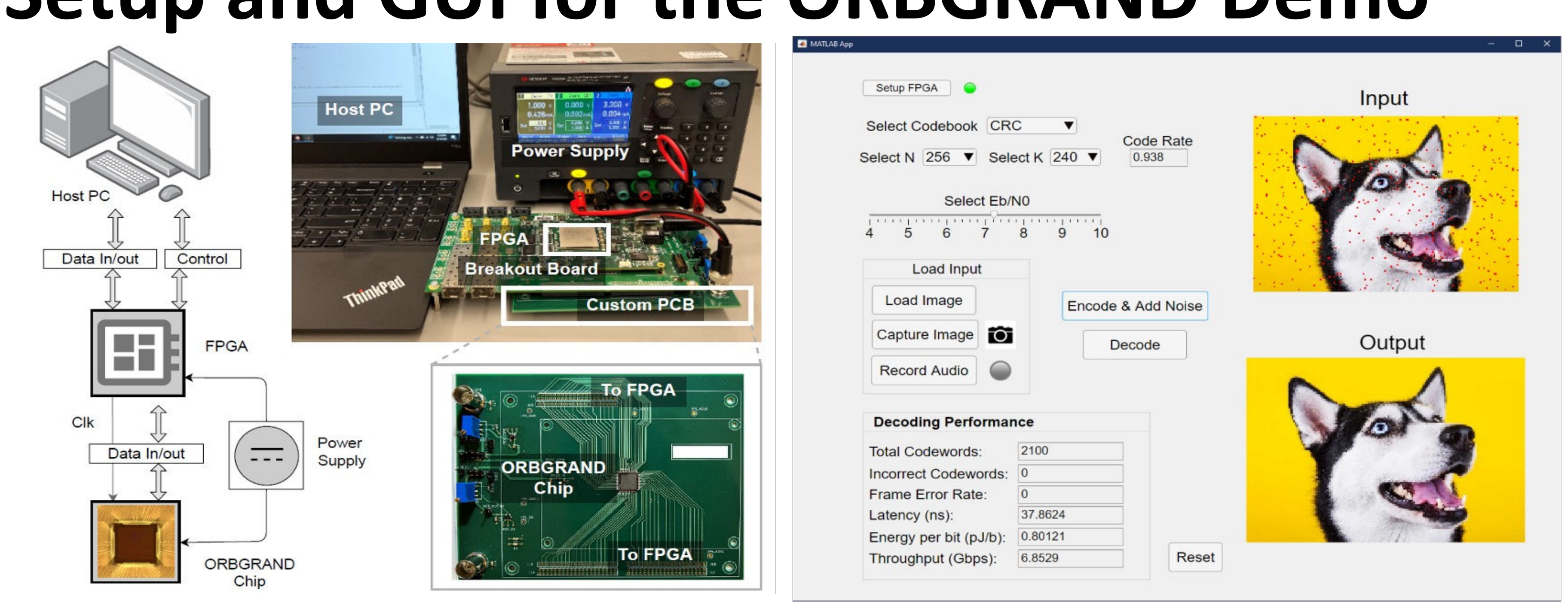
Hard-Detection Scenario



Soft-Detection Scenario



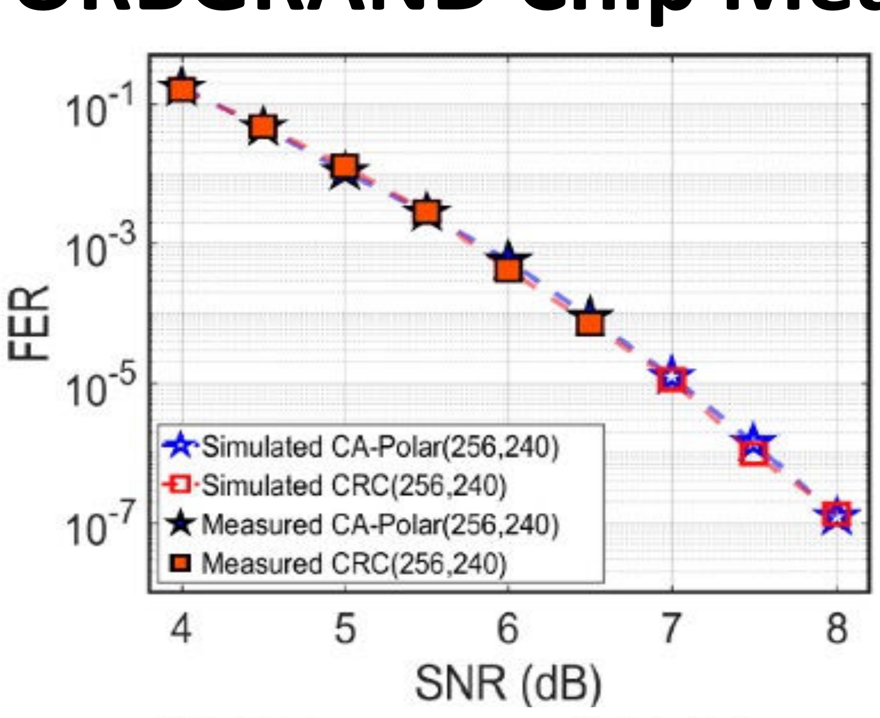
Setup and GUI for the ORBGRAND Demo

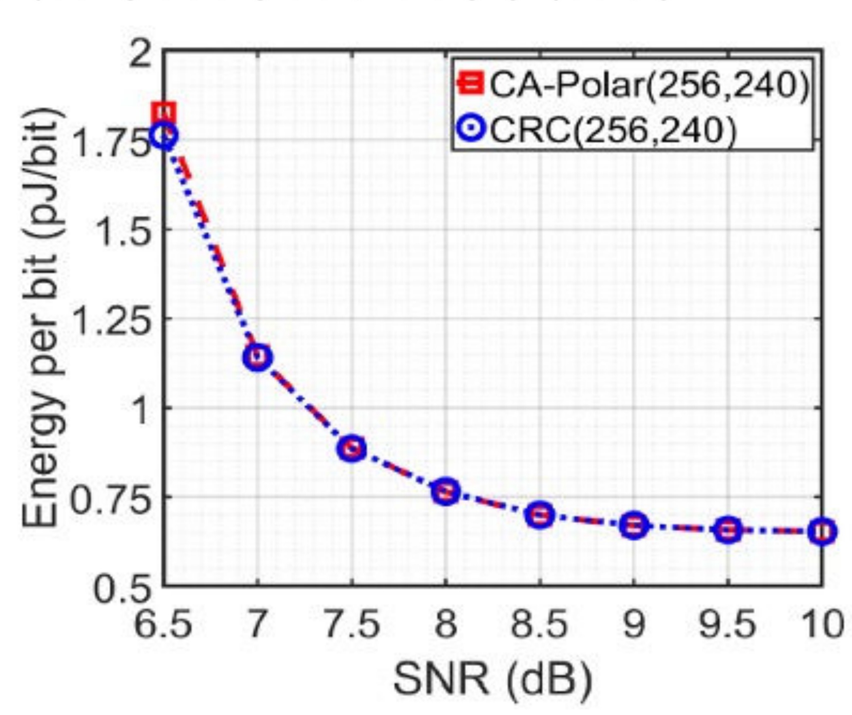


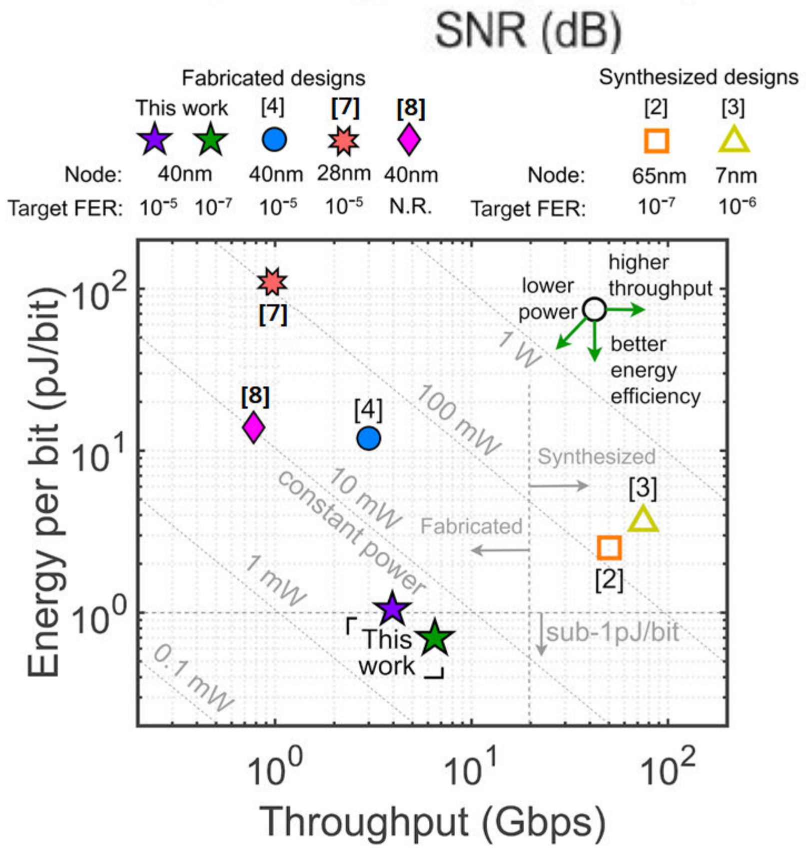
Broader Impacts

- Muriel Médard, Invited Speaker, "A Brief Tutorial on Guessing Random Additive Noise Decoding (GRAND)," 2023 IEEE ComSoc International School, Boston, June 2023
- M. Médard, Keynote Speaker, "Guessing Random Additive Noise Decoding (GRAND) or Universal Decoding Algorithm, and Relation to Signal Processing," IEEE LatinCom, Panama, November 2023
- M. Médard, Invited Speaker, "6G - What to Know Now," European Patent Office, November 2023
- R. T. Yazicigil, MediaTek (Semiconductor Research Corporation Member Company), "Decode Any Code with GRAND", November 2023
- R. T. Yazicigil, Lockheed Martin, "Decode Any Code with GRAND", December 2023
- K. R. Duffy, M. Médard, Invited Speaker, "GRAND: Guessing Random Additive Noise Decoding," Centrale Supélec Université of Paris-Saclay Seminar Series, Virtual, February 2024
- K. R. Duffy, Invited Speaker, "Guessing Random Additive Noise Decoding", ECE Distinguished Seminar Series, University of Michigan, March 2024
- K. R. Duffy, Invited Speaker, "Universal soft detection decoding in channels with memory - ORBGRAND-AI", Coding Theory for Modern Applications, Joint Mathematics Meetings, San Francisco, January 2024

ORBGRAND Chip Measurement Results







Reference	[1]	[2]	[3]	[4]
Sythesis/Fabricated	Fabricated	Synthesis	Synthesis	Fabricated
Technology (nm)	40	65	7	40
Code	CA-Polar/CRC (Universal)	CA-Polar (Universal)	BCH (Universal)	Polar
Algorithm	ORBGRAND	ORBGRAND	ORBGRAND	SCL
Code Length	Up to 256	128	127	Up to 1024
Supply (V)	1.0	0.9	0.5	0.9
Quantization (bits)	6	5	N.R.	6
Frequency (MHz)	90	454	616	430
Core Area (mm^2)	0.4	2.25	5.16	0.64
Target FER	10^{-7}	10^{-7}	10^{-6}	10^{-5}
Power (mW)	4.9	133	277.6	42.8
Energy per bit (pJ/bit)	0.76	2.57	3.52	13.2
Latency (ns)	40.0	2.47	40.6	N.R.
Throughput (Gbps)	6.5	51.8	78.85	3.25

Acknowledgments

This work was partially supported by Defense Advanced Research Projects Agency Contract number HR00112120008 and by National Science Foundation ECCS Award numbers 2128517 and 2128555.

References

[1] A. Riaz et al., "A Sub-0.8pJ/b 16.3Gbps/mm2 Universal Soft-Detection Decoder Using ORBGRAND in 40nm CMOS," in IEEE ISSCC, 2023
[2] S. M. Abbas et al., "High-Throughput and Energy-Efficient VLSI Architecture for Ordered Reliability Bits GRAND," IEEE TVLSI Systems, 2022
[3] C. Condo, "A Fixed Latency ORBGRAND Decoder Architecture With LUT-Aided Error-Pattern Scheduling," IEEE Transactions on Circuits and Systems, 2022
[4] Y. Tao, et al., "A Configurable Successive-Cancellation List Polar Decoder Using Split-Tree Architecture," IEEE JSSCC, 2021
[5] K. R. Duffy et al., "Ordered Reliability Bits Guessing Random Additive Noise Decoding," IEEE Transactions on Signal Processing, 2022
[6] F. Ercan et al., "GRAND-EDGE: A Universal, Jamming-Resilient Algorithm with Error-and-Erasure Decoding," IEEE ICC, 2023
[7] D. Kam, et al., "A 1.1μs 1.56Gb/s/mm2 Cost-Efficient Large-List SCL Polar Decoder Using Fully-Reusable LLR Buffers in 28nm CMOS Technology," IEEE Symposium on VLSI Technology and Circuits, 2022.
[8] C. -C. Teng, et al., "An Ultra-Low Latency 7.8–13.6 pJ/b Reconfigurable Neural Network-Assisted Polar Decoder with Multi-Code Length Support," IEEE Symposium on VLSI Circuits, 2020.