SWIFT: Advancing Coexistence through a Cross-Layer Design Platform with an Adaptive Frequency-Selective Radio Front-End and Digital Algorithms

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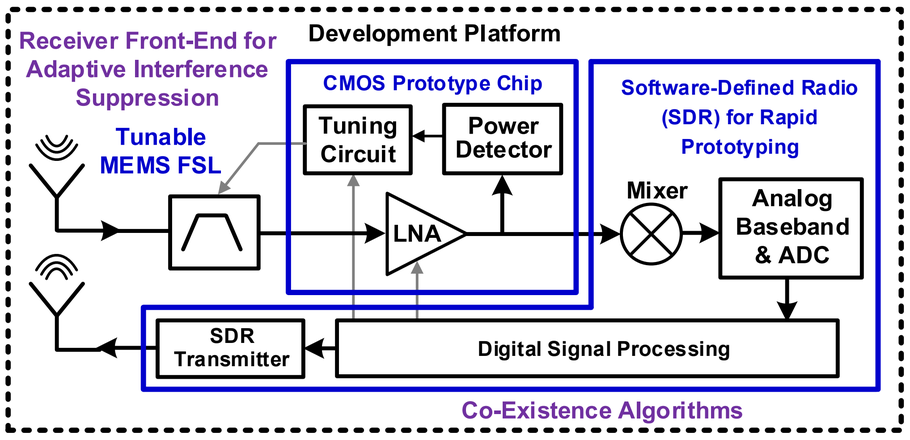
Overview



Envisioned platform for the co-design of tunable MEMS frequency selective limiters (FSLs) for interference suppression, adaptable low-power CMOS front-end circuits, and digital algorithms.

This research aims to create a platform and first hardware prototypes for the co-design of next-generation RF receivers with the ability to suppress both in-channel and adjacent channel interferers without compromising the reception of desired signals. Frequency selective limiters (FSLs) will be designed and fabricated, which can intrinsically distinguish and attenuate interference characterized by power levels higher than a certain threshold. The research utilizes this fundamental capability through the development of fully integrated microelectromechanical system (MEMS) FSLs that can be manufactured with complementary metal-oxide-semiconductor (CMOS) process compatibility, and that can be deliberately tuned by analog CMOS circuits towards accomplishing the best possible digital signal processing results when operating in crowded spectral environments. To broaden the benefits across wireless system layers, digital coexistence algorithms and adaptive analog front-end circuits will be conceived to strategically tune the operating points of the FSLs and of the receiver circuits towards the highest communication quality.

Project Summary

Goals

- Realization of FSLs with new monolithically integrated resonators having high quality factors (Q > 2,000). The acoustic properties of Aluminum Scandium Nitride (AlScN) thin-films and the ferroelectric properties of Hafnium Zirconium Oxide (HZO) atomic layers will be leveraged.
- Co-development of AlScN/HZO components with custom-designed analog circuits to achieve adaptive characteristics based on detected power levels, allowing to continuously optimize signal processing characteristics to changes in the surrounding electromagnetic spectrum.
- Design and fabrication of MEMS FSLs achieving 50dB interference suppression combined with CMOS signal power detectors and tuning circuits consuming less than 50µW while converging in less than 10µs.
- Creation of algorithms to enhance coexistence with the ability to transmit waveforms in adjacent channels with very narrow guard bands. Incorporation of software-defined radios (SDRs) for fast prototyping and testing.

Approach

- Integrated FSL design using AlScN two-dimensional-mode resonators (2DMRs) to form two parametric frequency dividers (PFDs) and a wideband 90° Hybrid Coupler (HC), leveraging board-level PFD design methods.
- Analog circuits and digital processing will enable real-time reconfiguration of the FSL and of the low-noise amplifier's operating conditions based on monitoring under varying interference conditions. The tuning will optimize interference suppression within 1-30MHz of the center frequency.
- General optimization for communication around 2.4GHz with channel spacing in the 2-5MHz range to allow proof-of-concept with Bluetooth Low Energy and ZigBee.

Intellectual Merit

- This research is establishing a framework for the co-design of RF front-ends with resilience to interference by leveraging the distinct features of CMOS circuits, AlScN/HZO components, digital algorithms and real-time calibrations.
- The outcomes will strengthen the resilience of wireless devices to both in-band and out-of-band interference, leading to adaptive radios for more efficient use of the available radio spectrum.
- A prototyping platform will be constructed to develop digital coexistence algorithms for cross-layer interference resilience.

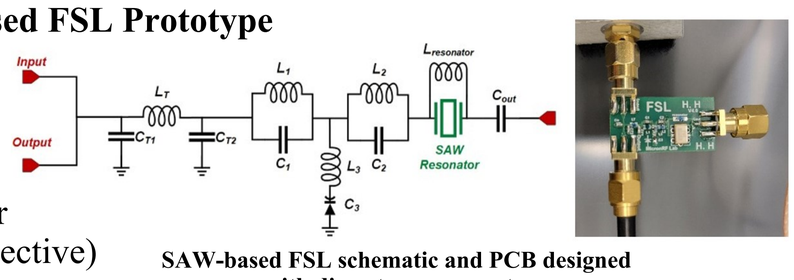
Broader Impacts

- The proposed research addresses the need to make low-power wireless receivers in IoT applications more immune to co-site interference and jamming.
- The design techniques will form the foundation for a new class of adaptive wireless systems with automatically tuned MEMS passives and analog circuits, which are digitally-controlled based on interference conditions.

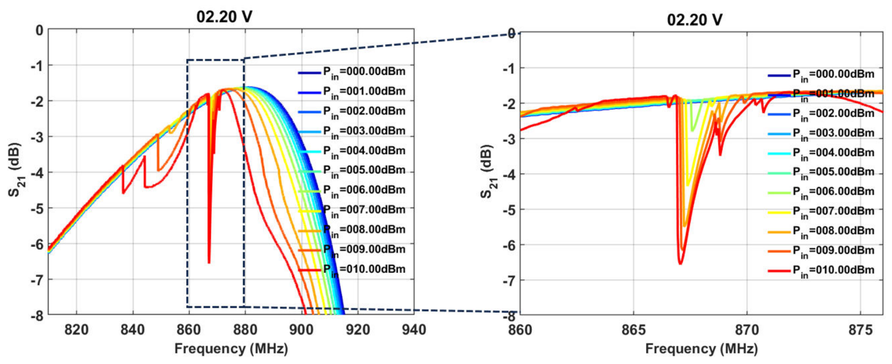
Recent Research Progress

Demonstration of a SAW-based FSL Prototype

- Design and fabrication of a proof-of-concept PCB
- Operation around 866 MHz
- High resonator quality factor (Q ≈ 10,000) → narrow (selective) and deep parametric notch
- The systematic analysis and design methodology will enable to design FSLs with different acoustic devices and frequency ranges.



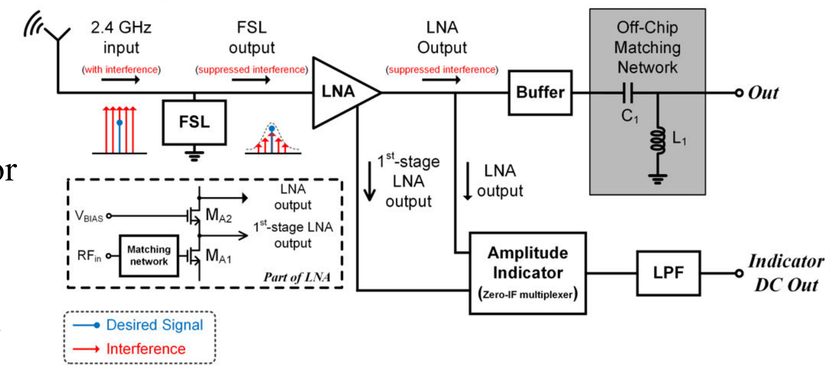
SAW-based FSL schematic and PCB designed with discrete components.



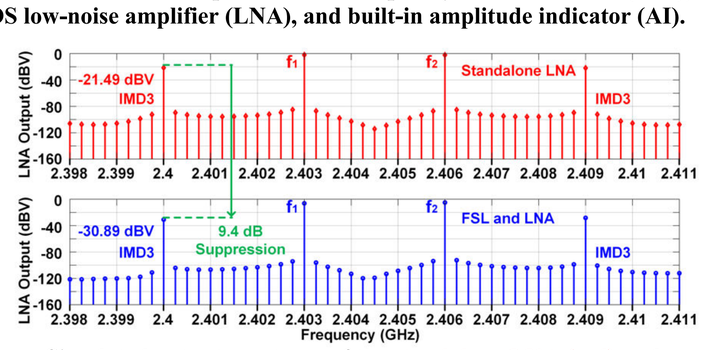
Measured transmission response (S_{21}) of the SAW-based FSL for multiple input power levels. The SAW resonator has a resonance frequency of ~433 MHz, which generates a parametric notch at twice of its resonance frequency (i.e., ~866 MHz) for interference suppression.

Low-Noise Amplifier (LNA) Co-Design and Simulation

- 2.4 GHz CMOS LNA: Designed with built-in power detection to monitor interference suppression
- An FSL simulation model was created and validated with measurements of a 2.4 GHz prototype.
- Simulation results show that the modeled FSL can provide 9.4 dB reduction of third-order intermodulation distortion (IMD3) components.



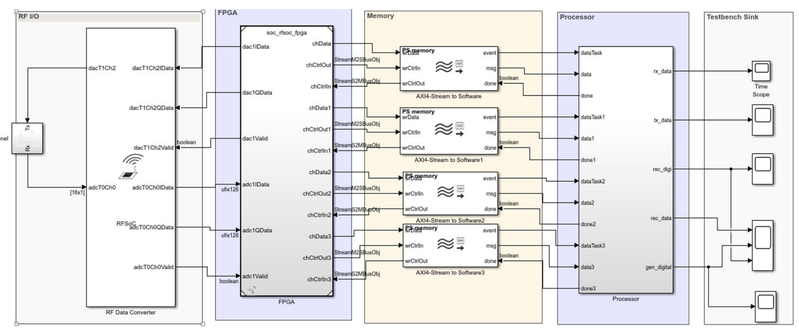
RF front-end under development with a frequency selective limiter (FSL), CMOS low-noise amplifier (LNA), and built-in amplitude indicator (AI).



Simulated output spectrum of the standalone LNA (red) and the FSL/LNA combination (blue) from a test with two -10 dBm (-23 dBV) interference tones at 2.403 and 2.406 GHz.

Communication Algorithm Development for Xilinx RFSoC Implementations

- The Xilinx RFSoC ZCU111 and ZCU216 were investigated as a prototyping platform for the communication algorithms in the 2.4GHz radio band, especially for the Bluetooth Low Energy (BLE) protocol.
- RFSoC design flow based on Matlab and Vivado:
  - Matlab HDL Coder enables high-level design for FPGAs, SoCs, ASICs. (use of toolboxes for SDR design with intuitive simulations & sign. proc.)
  - SoC Blockset used for performance simulations and analysis of algorithms on programmable SoCs and ASICs.



BLE algorithm in Matlab SoC Blockset

M. Yan, H. M. E. Hussein, C. Cassella, M. Rinaldi, and M. Onabajo, "Design and analysis of an on-chip current-driven CMOS parametric frequency divider," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 70, no. 5, pp. 1893-1906, May 2023.

H. Hussein, M. A. A. Ibrahim, M. Rinaldi, M. Onabajo, and C. Cassella, "Reflective parametric frequency selective limiters with sub-dB loss and µWatts power thresholds," *IEEE Trans. on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2989-3000, June 2021.

Future Work

- Design optimization, fabrication and testing of 2.4GHz MEMS FSLs
- Tape-out and testing of the 2.4 GHz LNA with an on-chip interference suppression indicator in 65nm CMOS technology
- Experimental BLE transceiver algorithm verification with the RFSoC hardware
- Development of FPGA-based performance optimization and algorithms to enhance interference suppression and co-existence